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PTO/SB/05 (12/97)

Approved for use through 09/30/00. OMB 0651-0032

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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**UTILITY PATENT APPLICATION TRANSMITTAL**  
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 042390.P9043 Total Pages 2  
First Named Inventor or Application Identifier Ganesh Subramaniyam  
Express Mail Label No. EL617210509US

ADDRESS TO: Assistant Commissioner for Patents  
Box Patent Application  
Washington, D. C. 20231

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form  
(Submit an original, and a duplicate for fee processing)
2. X Specification (Total Pages 18)  
(preferred arrangement set forth below)
  - Descriptive Title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claims
  - Abstract of the Disclosure
3. x Drawings(s) (35 USC 113) (Total Sheets 4)
4.    Oath or Declaration (Total Pages       )
  - a.    Newly Executed (Original or Copy)
  - b.    Copy from a Prior Application (37 CFR 1.63(d))  
(for Continuation/Divisional with Box 17 completed) (**Note Box 5 below**)
  - i.    DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5.    Incorporation By Reference (useable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6.    Microfiche Computer Program (Appendix)

09669034-092500

7.            Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)

a.            Computer Readable Copy

b.            Paper Copy (identical to computer copy)

c.            Statement verifying identity of above copies

8. ☐ Assignment Papers (cover sheet & documents(s))
9. ☐ a. 37 CFR 3.73(b) Statement (where there is an assignee)  
☐ b. Power of Attorney
10. ☐ English Translation Document (if applicable)
11. ☐ a. Information Disclosure Statement (IDS)/PTO-1449  
☐ b. Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☐ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ☐ a. Small Entity Statement(s)  
☐ b. Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. ☐ Other: \_\_\_\_\_

18. **Correspondence Address**

Customer Number or Bar Code Label \_\_\_\_\_  
 (Insert Customer No. or Attach Bar Code Label here)

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jc813 U.S. PTO  
09/669034  
09/25/00

## FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT (\$) 822.00

**Complete if Known:**

Application No. Unknown  
Filing Date Herewith  
First Named Inventor Ganesh Subramaniyam  
Group Art Unit \_\_\_\_\_  
Examiner Name \_\_\_\_\_  
Attorney Docket No. 042390.P9043

**METHOD OF PAYMENT (check one)**

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number 02-2666  
Deposit Account Name \_\_\_\_\_

- ☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

2. ☒ Payment Enclosed:

☒ Check  
\_\_\_\_ Money Order  
\_\_\_\_ Other

**FEE CALCULATION**

**1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
101	690	201	345	Utility application filing fee	<u>690.00</u>
106	310	206	155	Design application filing fee	_____
107	480	207	240	Plant filing fee	_____
108	690	208	345	Reissue filing fee	_____
114	150	214	75	Provisional application filing fee	_____
SUBTOTAL (1)					<u>\$ 690.00</u>

**2. EXTRA CLAIM FEES**

		Extra Claims	Fee from below	Fee Paid
Total Claims	<u>23</u>	- 20** = <u>3</u>	X <u>18.00</u>	= <u>54.00</u>
Independent Claims	<u>4</u>	- 3** = <u>1</u>	X <u>78.00</u>	= <u>78.00</u>
Multiple Dependent				= _____

\*\*Or number previously paid, if greater; For Reissues, see below.

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) \$ 132.00

01/10/2000

- 1 -

PTO/SB/17 (6/99)

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.  
See Forms PTO/SB/09-12

**FEE CALCULATION (continued)****3. ADDITIONAL FEES**

<u>Large Entity</u>		<u>Small Entity</u>		<u>Fee Description</u>	<u>Fee Paid</u>
<u>Fee Code</u>	<u>Fee (\$)</u>	<u>Fee Code</u>	<u>Fee (\$)</u>		
105	130	205	65	Surcharge - late filing fee or oath	_____
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	_____
139	130	139	130	Non-English specification	_____
147	2,520	147	2,520	For filing a request for reexamination	_____
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	_____
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	_____
115	110	215	55	Extension for response within first month	_____
116	380	216	190	Extension for response within second month	_____
117	870	217	435	Extension for response within third month	_____
118	1,360	218	680	Extension for response within fourth month	_____
128	1,850	228	925	Extension for response within fifth month	_____
119	300	219	150	Notice of Appeal	_____
120	300	220	150	Filing a brief in support of an appeal	_____
121	260	221	130	Request for oral hearing	_____
138	1,510	138	1,510	Petition to institute a public use proceeding	_____
140	110	240	55	Petition to revive unavoidably abandoned application	_____
141	1,210	241	605	Petition to revive unintentionally abandoned application	_____
142	1,210	242	605	Utility issue fee (or reissue)	_____
143	430	243	215	Design issue fee	_____
144	580	244	290	Plant issue fee	_____
122	130	122	130	Petitions to the Commissioner	_____
123	50	123	50	Petitions related to provisional applications	_____
126	240	126	240	Submission of Information Disclosure Stmt	_____
581	40	581	40	Recording each patent assignment per property (times number of properties)	_____
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	_____
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	_____

Other fee (specify) \_\_\_\_\_

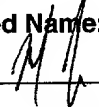
Other fee (specify) \_\_\_\_\_

**SUBTOTAL (3) \$ 0**

\*Reduced by Basic Filing Fee Paid

**SUBMITTED BY:**

Typed or Printed Name: Mark L. Watson

Signature  Date 9/25/00

Reg. Number 46,322 Deposit Account User ID \_\_\_\_\_  
(complete if applicable)

UNITED STATES PATENT APPLICATION

for

METHOD AND APPARATUS FOR MAINTAINING THE TEMPERATURE OF A  
MICROPROCESSOR USING A FIRMWARE ASSISTED INTERRUPT MECHANISM

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File No.: 042390.P9043

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September 25, 2000  
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

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# METHOD AND APPARATUS FOR MAINTAINING THE TEMPERATURE OF A MICROPROCESSOR USING A FIRMWARE ASSISTED INTERRUPT MECHANISM

## FIELD OF THE INVENTION

The present invention relates to computer systems; more particularly, the present invention relates to lowering and maintaining the temperature of a microprocessor die below a burnout temperature.

## 5 BACKGROUND

Throughout the history of microcomputers there has been a motivation to increase the performance of microprocessors. However, with the constant increase in microprocessor performance, there is typically an increase in the magnitude of power consumed by the microprocessor. Due to the increase in power consumption, the run time temperature of the die of a microprocessor may exceed a safe threshold value.

Various methods currently exist to reduce the run time temperature of microprocessors. One such method is to modulate the processor clock. Another method is to modulate the processor clock frequency. However, these methods complicate the hardware design implementation, validation and also decrease the performance of a microprocessor. Yet another solution for cooling the run time temperature of a microprocessor is to shut down the microprocessor and reboot the computer system at a later time. However having to shut down the computer is obviously disadvantageous as it increases the down time of the system. Therefore, it would be advantageous to develop a more efficient method of maintaining the run time temperature of a microprocessor.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various  
5   embodiments of the invention. The drawings, however, should not be taken to  
limit the invention to the specific embodiments, but are for explanation and  
understanding only.

**Figure 1** is a block diagram of one embodiment of a computer system;

**Figure 2** is a block diagram of one embodiment of a microprocessor; and

10   **Figure 3** is a flow diagram for one embodiment of controlling the  
temperature of a microprocessor.

## DETAILED DESCRIPTION

A method and apparatus for maintaining the temperature of a microprocessor is described. In the following detailed description of the present invention numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

**Figure 1** is a block diagram of one embodiment of a computer system 100. Computer system 100 includes a central processing unit (processor) 105 coupled to processor bus 110. In one embodiment, processor 105 is a processor in the Pentium® family of processors including the Pentium® II family and mobile Pentium® and Pentium® II processors available from Intel Corporation of Santa Clara, California. Alternatively, other processors may be used. Processor 105 may include a first level (L1) cache memory (not shown in **Figure 1**).

According to one embodiment, processor 105 operates in either a full dispersal mode or a single dispersal mode. In the full dispersal mode, processor 105 executes multiple instructions at a time. According to one embodiment, processor 105 executes six instructions at a time. In the single dispersion mode, processor 105 executes one instruction at a time. According to a further



embodiment, processor 105 transitions from the full dispersion mode to the single dispersion mode upon the die temperature of processor 105 exceeding a predetermined temperature threshold.

In yet a further embodiment, processor 105 operates according to an artificial activity mode. The artificial activity mode minimizes current spikes (e.g.,  $\frac{di}{dt}$  spikes) within processor 105 by maintaining a minimum level of activity within processor 105. For example, if the activity (e.g., instructions received and/or executed) falls below a predetermined threshold, simulated instructions are received at processor 105 for processing. The simulated instructions may be received from the L1 cache memory, a floating point unit, integer unit or any other device within processor 105 or computer system 100. The results of the simulated instructions are disregarded after processing. According to one embodiment, the minimum level of activity within processor 105 is seventy percent of processor 105 capacity. However in other embodiments, the minimum level of activity within processor 105 may be other percentages of processor 105 capacity.

In one embodiment, processor 105 is also coupled to cache memory 107, which is a second level (L2) cache memory, via dedicated cache bus 102. The L1 and L2 cache memories can also be integrated into a single device. Alternatively, cache memory 107 may be coupled to processor 105 by a shared bus. Cache memory 107 is optional and is not required for computer system 100.

Chip set 120 is also coupled to processor bus 110. In one embodiment, chip set 120 is the 440BX chip set available from Intel Corporation; however, other chip sets can also be used. Chip set 120 may include a memory controller for controlling a main memory 113. Further, chipset 220 may also include an Accelerated Graphics Port (AGP) Specification Revision 2.0 interface 320

developed by Intel Corporation of Santa Clara, California. AGP interface 320 is coupled to a video device 125 and handles video data requests to access main memory 113.

Main memory 113 is coupled to processor bus 110 through chip set 120.

5 Main memory 113 and cache memory 107 store sequences of instructions that are executed by processor 105. The sequences of instructions executed by processor 105 may be retrieved from main memory 113, cache memory 107, or any other storage device. Additional devices may also be coupled to processor bus 110, such as multiple processors and/or multiple main memory devices. Computer  
10 system 100 is described in terms of a single processor; however, multiple processors can be coupled to processor bus 110. Video device 125 is also coupled to chip set 120. In one embodiment, video device 125 includes a video monitor such as a cathode ray tube (CRT) or liquid crystal display (LCD) and necessary support circuitry.

15 Processor bus 110 is coupled to system bus 130 by chip set 120. In one embodiment, system bus 130 is a Peripheral Component Interconnect (PCI) bus adhering to a Specification Revision 2.1 bus developed by the PCI Special Interest Group of Portland, Oregon; however, other bus standards may also be used. Multiple devices, such as audio device 127, may be coupled to system bus 130.

20 Bus bridge 140 couples system bus 130 to secondary bus 150. In one embodiment, secondary bus 150 is an Industry Standard Architecture (ISA) Specification Revision 1.0a bus developed by International Business Machines of Armonk, New York. However, other bus standards may also be used, for example Extended Industry Standard Architecture (EISA) Specification Revision  
25 3.12 developed by Compaq Computer, et al. Multiple devices, such as hard disk 153 and disk drive 154 may be coupled to secondary bus 150. Other devices, such as cursor control devices (not shown in **Figure 1**), may be coupled to

secondary bus 150.

According to one embodiment, a basic input output system (BIOS) 155 is coupled to secondary bus 150. BIOS 155 includes arrays of programmable AND gates and predefined OR gates that store a set of routines which provide an interface between the operating system and components of computer system 100. According to one embodiment, BIOS 155 transmits signals to processor 105 to initiate the generation of artificial activity at processor 105. In one embodiment, BIOS 155 is programmable array logic (PAL). However, one of ordinary skill in the art will appreciate that other devices may be used to implement BIOS 155.

According to one embodiment, processor 105 includes power management logic to prevent prolonged operation at excess temperatures. During the run time of computer system 105, the power consumed at processor 105 may exceed 130 watts. Such power consumption may cause processor 105 to overheat and lead to the eventual burnout of processor 105. **Figure 2** is a block diagram of one embodiment of temperature monitoring logic within processor 105.

Referring to **Figure 2**, processor 105 includes a thermal sensor 210, an analog to digital converter (ADC) 220, a filter 230, interrupt generating hardware 240, instruction execution unit 250, and artificial activity generator 260. In addition, processor 105 is coupled to an interrupt handler 270. According to one embodiment, sensor 210 is an analog sensor that continuously monitors the temperature of processor 105 during the operation of computer system 100. ADC 220 is coupled to sensor 210 and converts an analog temperature value received from sensor 210 to a one-bit digital signal.

According to one embodiment, ADC 220 transmits a low logic level (e.g., logic 0) if the temperature value received is below a predetermined threshold and transmits a high logic level (e.g., logic 1) if the temperature value is above

the predetermined threshold. One of ordinary skill in the art will appreciate that the combination of sensor 210 and ADC 220 may be replaced by a digital sensor in other embodiments.

Filter 230 is coupled to ADC 220. Filter 230 is a digital filter that removes temperature noise conditions for a predetermined number of clock cycles. According to one embodiment, filter 230 determines how long the die temperature is above or below the predetermined threshold before initiating a high temperature or normal temperature interrupt, respectively. According to a further embodiment, digital filter 230 removes noise conditions for two clock cycles. In yet a further embodiment, the number of predetermined clock cycles may be programmed into digital filter 230.

Interrupt generating hardware 240 is coupled to filter 230. Interrupt generating hardware 240 generates a high temperature (HITEMP) interrupt upon the die temperature of processor 105 exceeding the predetermined threshold temperature, subject to the operations of filter 230. In addition, interrupt generating hardware 240 generates a normal temperature (NORMTEMP) interrupt upon the die temperature of processor 105 cooling below the predetermined threshold temperature. In one embodiment, a high logic level is transmitted by interrupt generating hardware 240 as the HITEMP interrupt. Further, a low logic level is transmitted by interrupt generating hardware 240 as the NORMTEMP interrupt. One of ordinary skill in the art will recognize that the operation of ADC 220 may be reversed.

Instruction execution unit 250 determines the dispersal mode in which processor 105 operates. In one embodiment, instruction execution unit 250 causes processor 105 to operate in the full dispersal mode whenever the die temperature is below the predetermined threshold temperature. Conversely, execution unit 250 causes processor 105 to operate in the single dispersal mode

whenever the die temperature is above the predetermined threshold temperature.

Artificial activity generator 260 controls the artificial activity within processor 105. As described above, an artificial activity mode minimizes current spikes within processor 105 by maintaining a minimum level of activity. Artificial activity generator 260 determines the level of artificial activity that is generated at processor 105. According to one embodiment, artificial activity generator suspends artificial activity within processor 105 whenever the die temperature is above the predetermined threshold temperature.

Interrupt handler 270 is coupled to interrupt generating hardware 240, instruction execution unit 250 and artificial activity generator 260. In one embodiment, interrupt handler 270 receives the processor level interrupts HITEMP and NORMTEMP and causes the appropriate action to be taken. For example, upon receiving the HITEMP interrupt, interrupt handler 270 transmits a signal to instruction execution unit 250 causing processor 105 to transition from the full dispersal mode to the single dispersal mode. By placing processor 105 in the single dispersal mode, the utilization of components within processor 105 is reduced, resulting in the cooling of temperature within processor 105. Similarly, interrupt handler 270 causes processor 105 to transition back to the full dispersal mode upon receiving the NORMTEMP interrupt.

Further, interrupt handler 270 transmits signals to artificial activity generator to suspend and resume artificial activity depending upon the die temperature. According to one embodiment, interrupt handler 270 resides within BIOS 155. In a further embodiment, interrupt handler 270 may reside in main memory 113 upon startup of computer system 100. However, one of ordinary skill in the art will appreciate that interrupt handler 270 may be located elsewhere within computer system 100.

Figure 3 is a flow diagram for one embodiment of controlling the temperature of processor 105. At process block 305, processor 105 is operating in the full dispersal mode. As described above, the full dispersal mode features executing instruction streams at very high processor 105 utilization. At process block 310, it is determined whether the die temperature of processor 105 has exceeded the predetermined threshold. If the die temperature has not exceeded the predetermined threshold, control is returned to process block 305.

However, if the die temperature has exceeded the predetermined threshold, the HITEMP interrupt is generated at ADC 220, process block 315.

According to one embodiment, the execution of code within processor 105 is temporarily suspended after the HITEMP interrupt is generated. At process block 320, interrupt handler 270 causes processor 105 to cease operation in the artificial activity mode. By stopping artificial activity, processor 105 is permitted to fall below the predetermined minimum level of activity.

In addition, at process block 325, interrupt handler 270 causes processor 105 to transition from the full dispersal mode to the single dispersal mode. At process block 330, the execution of code within processor 105 continues in the single dispersion mode from the point at which it was suspended. As described above, the single dispersal mode clamps the maximum utilization of components within processor 105. As a result, the power consumed by processor 105 is limited. At process block 335, it is determined whether the die temperature of processor 105 continues to remain above the predetermined temperature threshold. If the temperature remains above the predetermined threshold, processor 105 is shut down, process block 340.

If, however, the die temperature of processor 105 falls below the predetermined threshold, the NORMTEMP interrupt is generated, process block 345. The execution of code within processor 105 is temporarily suspended after

the NORMTEMP interrupt is generated. At process block 350, interrupt service handler code within interrupt handler service 270 causes processor 105 to commence operation in the artificial activity mode. In addition, at process block 355, interrupt handler 270 causes processor 105 to transition from the single  
5 dispersal mode to the full dispersal mode. At process block 360, interrupt handler 270 causes the execution of code within processor 105 to continue in the full dispersion mode from the point at which it was suspended.

Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having  
10 read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.

## CLAIMS

What is claimed is:

- 1 1. A system comprising a central processing unit (CPU), wherein the CPU  
2 includes power management logic that that enables the CPU to operate in a first  
3 execution mode whenever the temperature of the CPU exceeds the  
4 predetermined threshold and operates in a second execution mode whenever the  
5 temperature of the CPU is below the predetermined threshold.
- 1 2. The system of claim 1 wherein the power management logic comprises:  
2 a thermal sensor;  
3 a digital filter coupled to the thermal sensor; and  
4 an interrupt generating hardware coupled to the digital filter, wherein the  
5 interrupt generating hardware generates a first interrupt whenever the  
6 temperature of the CPU exceeds the predetermined threshold and generates a  
7 second interrupt whenever the temperature of the CPU is below the  
8 predetermined threshold.
- 1 3. The system of claim 2 wherein the power management logic further  
2 comprises an analog to digital converter coupled between the thermal sensor and  
3 the digital filter.
- 1 4. The system of claim 2 further comprising programmable array logic  
2 (PAL), wherein the PAL includes an interrupt handler for receiving the first and  
3 second interrupts.



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1 5. The system of claim 4 wherein the power management logic further  
2 comprises:

3 an instruction execution unit coupled to the interrupt handler; and  
4 an artificial activity generator coupled to the interrupt handler.

1 6. The system of claim 5 wherein the instruction execution unit causes the  
2 CPU to operate in a full dispersal mode whenever the die temperature is below  
3 the predetermined threshold temperature and to operate in a single dispersal  
4 mode whenever the die temperature is above the predetermined threshold  
5 temperature.

1 7. The system of claim 5 wherein the artificial activity generator causes the  
2 CPU artificial activity generator to suspend artificial activity within the CPU  
3 whenever the die temperature is above the predetermined threshold  
4 temperature.

1 8. A method comprising:  
2 determining whether the temperature of a central processing unit (CPU)  
3 exceeds a predetermined threshold;  
4 generating a first interrupt if the temperature of the CPU exceeds the  
5 predetermined threshold; and  
6 transitioning from a first execution mode to a second execution mode.



5 generating a second interrupt if the CPU does not exceed the  
6 predetermined threshold after transitioning to the single instruction execution  
7 mode.

1 13. The method of claim 12 further comprising transitioning from the second  
2 execution mode to the first execution mode.

1 14. The method of claim 13 wherein the process of transitioning from the  
2 second execution mode to the first execution mode comprises:  
3 resuming the artificial activity mode; and  
4 transitioning from the single instruction execution mode to the full  
5 instruction execution mode.

1 15. The method of claim 12 wherein the first interrupt is a high temperature  
2 interrupt and the second interrupt is a normal temperature interrupt.

1 16. A central processing unit (CPU) comprising:  
2 a thermal sensor;  
3 an analog to digital converter coupled to the thermal sensor  
4 a digital filter coupled to the analog to digital converter; and  
5 an interrupt generating hardware coupled to the digital filter, wherein the  
6 interrupt generating hardware generates a first interrupt whenever the  
7 temperature of the CPU exceeds the predetermined threshold and generates a  
8 second interrupt whenever the temperature of the CPU is below the  
9 predetermined threshold.

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1 17. The CPU of claim 16 further comprising:

2 an instruction execution unit; and

3 an artificial activity generator.

1 18. The CPU of claim 17 wherein the instruction execution unit causes the

2 CPU to operate in a full dispersal mode whenever the die temperature is below

3 the predetermined threshold temperature and to operate in a single dispersal

4 mode whenever the die temperature is above the predetermined threshold

5 temperature.

1 19. The CPU of claim 16 wherein the artificial activity generator causes the

2 artificial activity generator to suspend artificial activity within the CPU

3 whenever the die temperature is above the predetermined threshold

4 temperature.

1 20. Power management logic comprising:

2 a thermal sensor;

3 an analog to digital converter coupled to the thermal sensor

4 a digital filter coupled to the analog to digital converter; and

5 an interrupt generating hardware coupled to the digital filter, wherein the

6 interrupt generating hardware generates a first interrupt whenever the

7 temperature a central processing unit (CPU) exceeds the predetermined

8 threshold and generates a second interrupt whenever the temperature of the

9 CPU is below the predetermined threshold.

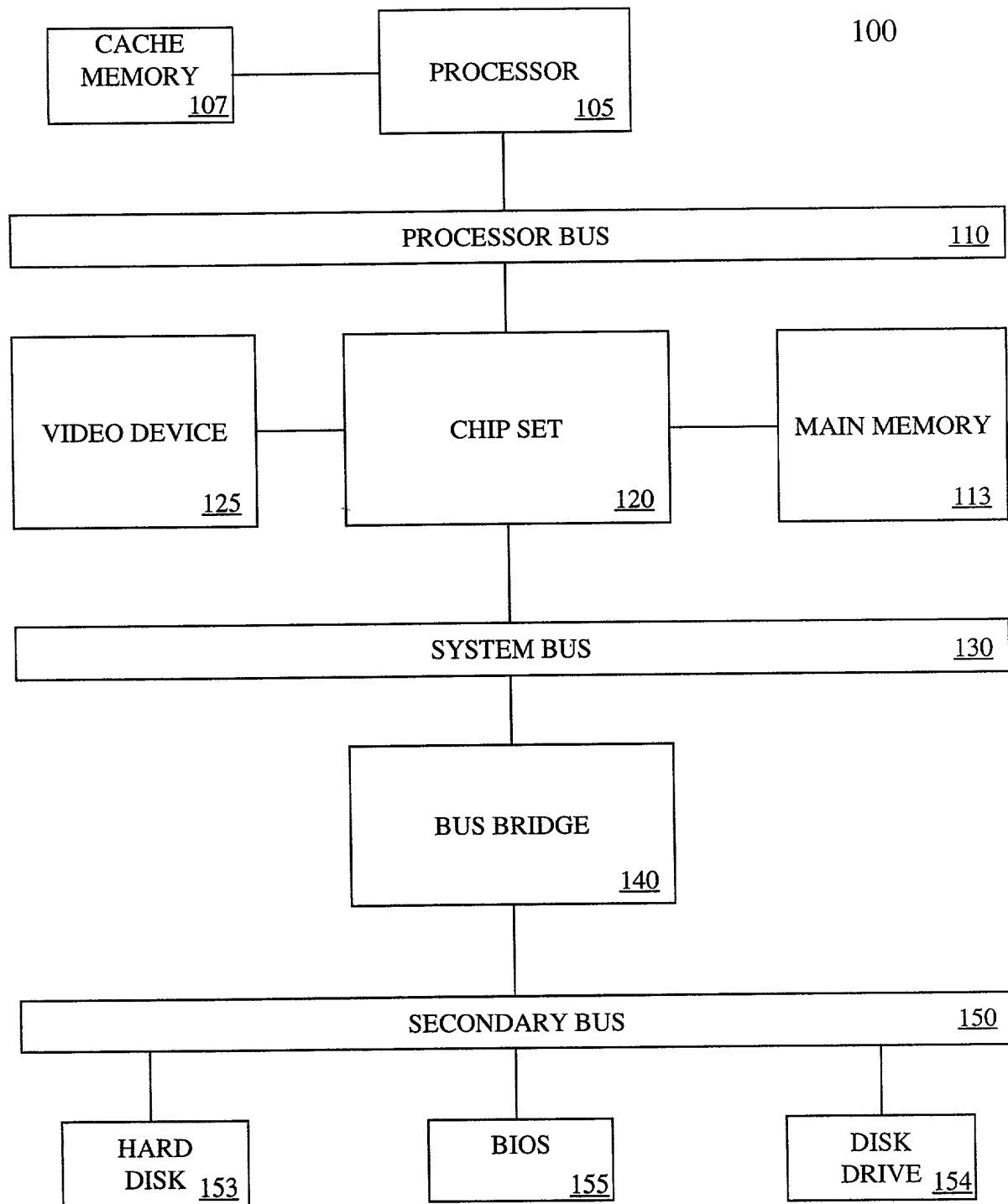
1 21. The power management logic of claim 20 further comprising:  
 2 an instruction execution unit; and  
 3 an artificial activity generator.

1 22. The power management logic of claim 20 wherein the instruction  
 2 execution unit causes the CPU to operate in a full dispersal mode whenever the  
 3 die temperature is below the predetermined threshold temperature and to  
 4 operate in a single dispersal mode whenever the die temperature is above the  
 5 predetermined threshold temperature.

1 23. The power management logic of claim 20 wherein the artificial activity  
 2 generator causes the artificial activity generator to suspend artificial activity  
 3 within the CPU whenever the die temperature is above the predetermined  
 4 threshold temperature.

## ABSTRACT

According to one embodiment, a method is disclosed. The method includes determining whether the temperature of a central processing unit (CPU) exceeds a predetermined threshold. In addition, the method includes generating  
5 a first interrupt if the temperature of the CPU exceeds the predetermined threshold and transitioning from a first execution mode to a second execution mode.



**FIGURE 1**

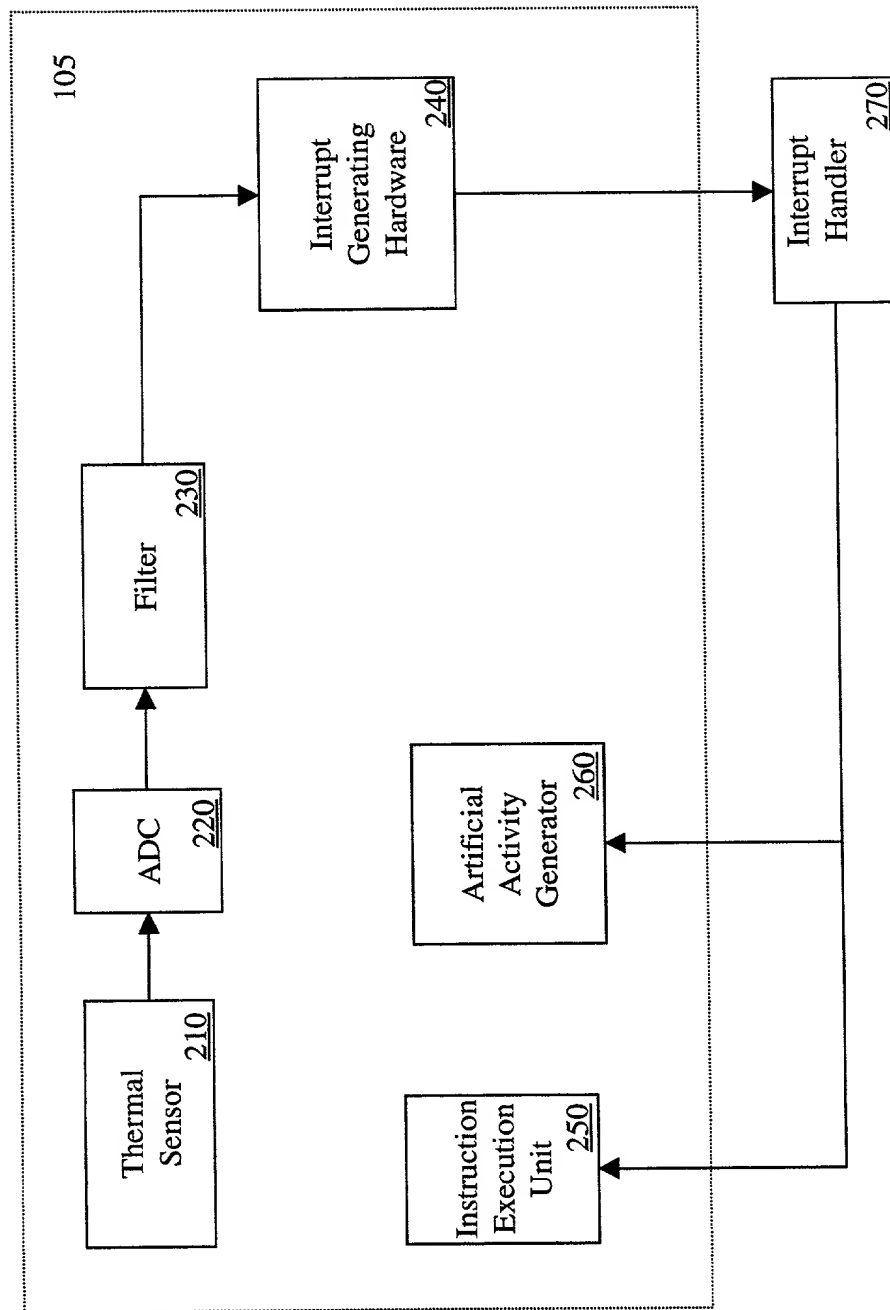


FIGURE 2



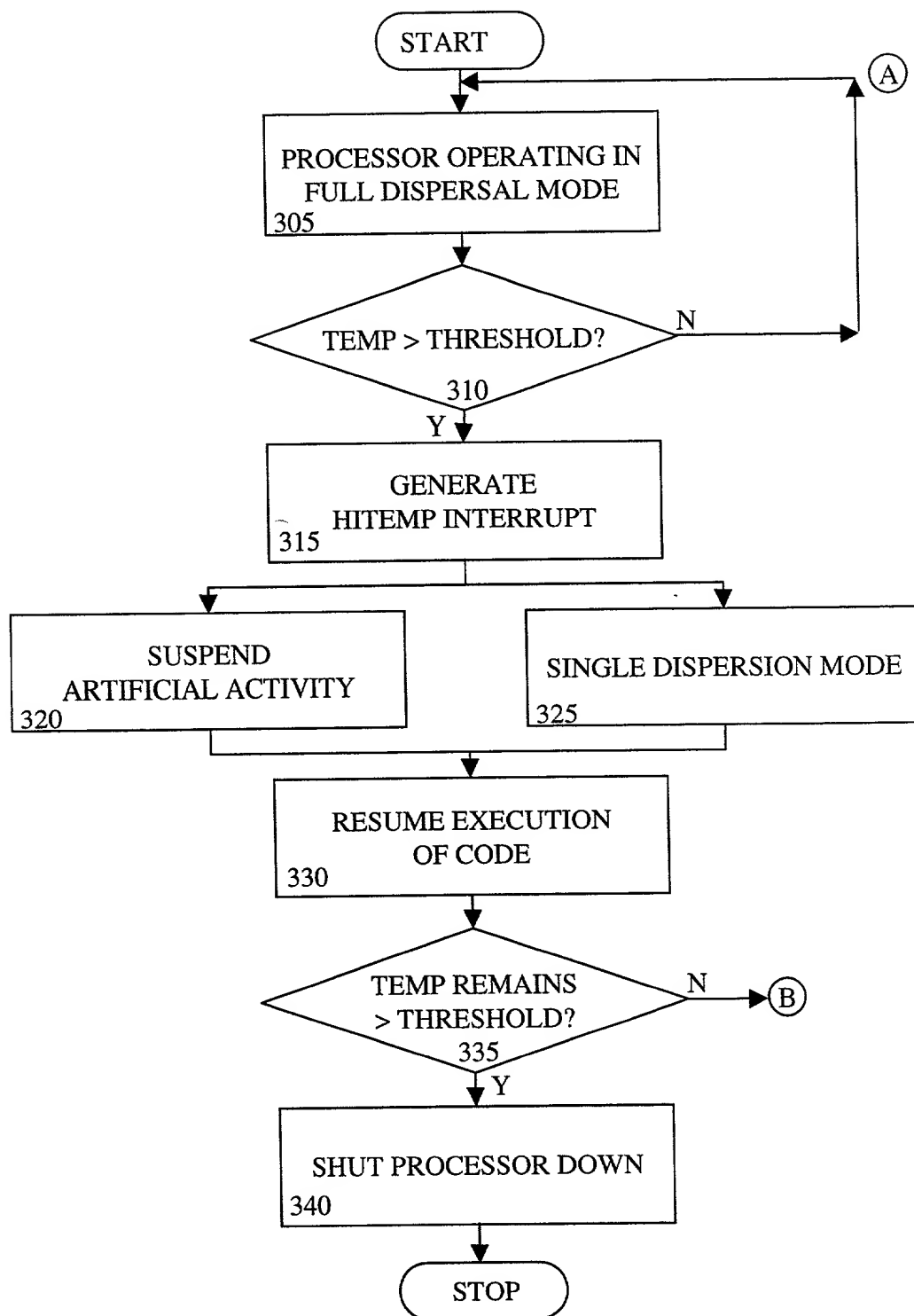
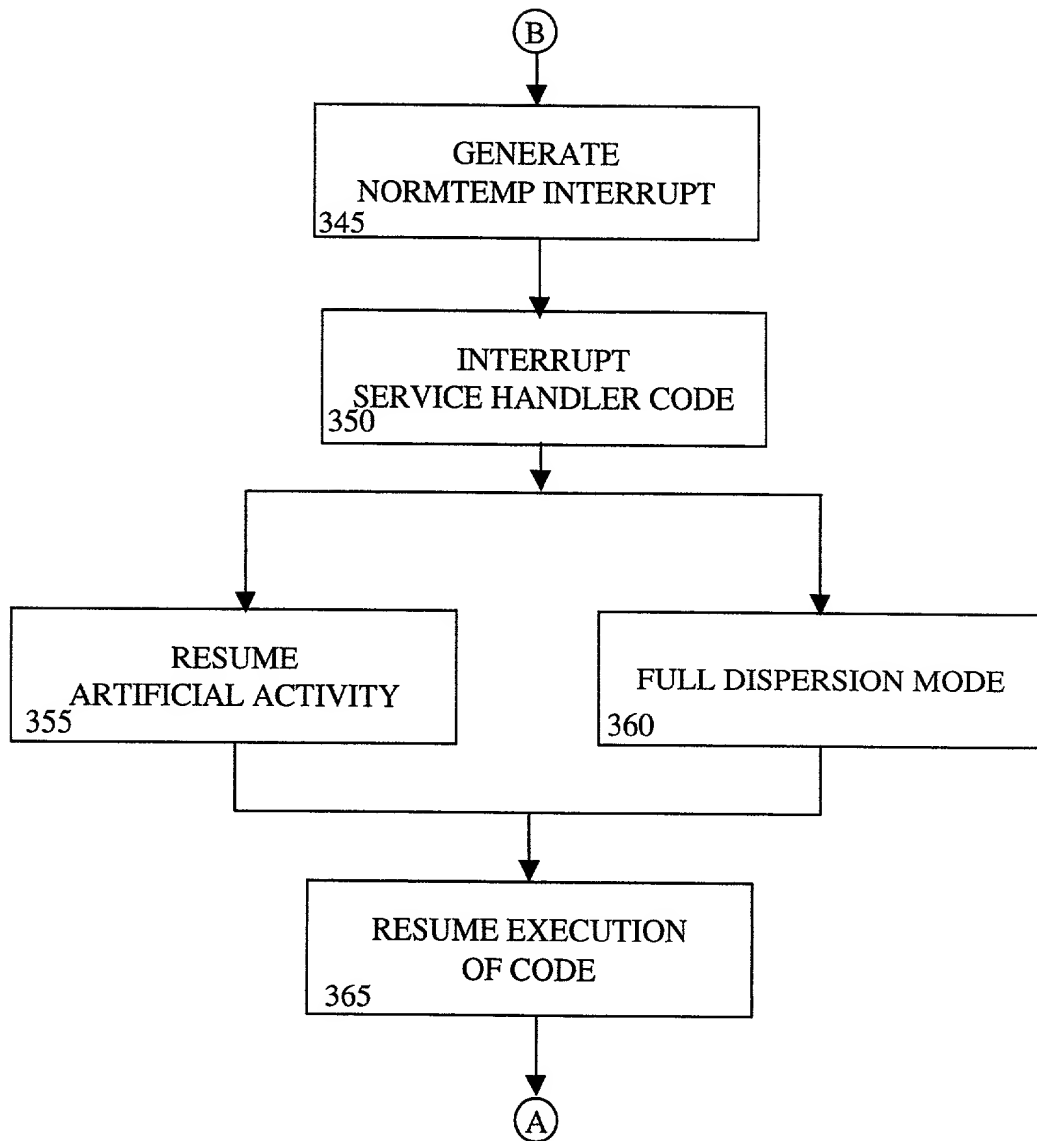


FIGURE 3A

005250"4E059390



**FIGURE 3B**